UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/516,675 | 06/22/2005 | Helge Betzinger | A36433 PCTUSA<br>066340.0125 | 6649 |

21003 7590 10/22/2007

BAKER BOTTS L.L.P.
30 ROCKEFELLER PLAZA
44TH FLOOR
NEW YORK, NY 10112-4498

| EXAMINER | |
|---|---|
| TSENG, CHENG YUAN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2184 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 10/22/2007 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

DLNYDOCKET@BAKERBOTTS.COM

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/516,675 | BETZINGER ET AL. | |
| | Examiner | Art Unit | |
| | Cheng-Yuan Tseng | 2184 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *8 and 10-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8 and 10-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

**DETAILED ACTION**

***Response to Amendment***

1. The objections to certain informalities in claims and specification have been withdrawn due to the amendment filed on October 5th, 2007.

2. The rejection under 35 USC 101 has been withdrawn due to the amendment filed on October 5th, 2007.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless - (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 8-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Pechanek et al. (U.S. Patent 6,101,592), hereinafter referring to as Pechanek'592.

Referring to claim 8, Pechanek'592 discloses a method for actuating function units in **a processor** (fig. 1A, processor

100), wherein **a configuration phase** (fig. 4A, translation process 400) involves **a series of primary instruction words** (fig. 4A, 15-bit compacted-1 instruction 401) that come from a translation of a program code being divided into **a series of instruction word parts** (fig. 4A, 32-bit ADD instruction 403), with a program cycle involving instruction words which **actuate** (col. 3, lines 43-46, and fig. 1A, 1B, the compact instruction is "instruction words" in which, with operating codes, they active each PE's ALU within processor 100) the processor being constructed in the full instruction word length to form **a Very Long Instruction Word VLIW** (fig. 5, VLIW is instruction of store+load+alu instructions+mau instruction+dsu instructions) and being buffer-stored in **an instruction word memory cache** (fig. 5, VIM), the method comprising:

a first step that involves **a primary instruction word** (fig. 4A, 15-bit compacted-1 instruction 401) being divided, in the **configuration phase** (fig. 4A, ALU translation process 400), into the series of **a particular number of instruction word parts** (fig. 4A, 32-bit ADD instruction 403) which are used for constructing **a respective VLIW** (fig. 5, VLIW is instruction of store+load+alu instructions+mau instruction+dsu instructions,or fig. 1A, instruction native to SP/PE0, PE1, PE2, and PE3) during the execution phase, with **a respective first and second Function**

**Instruction Word FIW part**(fig. 6, first FIW is bits 29-15, second is bits 14-0), being **preceded** (fig. 6D, Translation Process 670, 680) with **an associated first or second operating code** (fig. 3A, bits 27-24 is opcode), which thus **determines** (fig. 6D, VIMOffs in 657/655) how the cache's memory location taken up (fig. 7A, VIM Load/Store Control coupled to iVIM Memory VIM as cache) by the respective FIW is handled in the execution phase (fig. 8, execute units 840/842/844/846/848),

wherein the respective first and second operating code (fig. 3A, bits 24-27) are respectively followed by **an associated first and second tag** (fig. 3A, bits 28-29) that represent the information regarding which of **a first and a second FU** (fig. 3A, bits 24-27) actuates (col. 3, lines 43-46, and fig. 1A, 1B, the compact instruction is "instruction words" in which, with operating codes, they active each PE's ALU within the processor 100) the respective FIW (col. 3, lines 43-46, and fig. 1A, 1B),

wherein, the respective first and second operating code (fig. 3A, bits 24-27) and their associated first or second tag (fig. 3A, bits 28-29) are **combined** (fig. 2-5, instructions and tags are combined) with the respective first and second FIWs to form the **first and second Tagged Very Long Instruction Word TVLIW** (fig. 5, Compacted-1 Instructions) containers all of which represent the TVLIW; and

a second step that involves the respective TVLIW being converted into **an Head Very Long Instruction Word HVLIW** (col. 17, claim 6, HVLIW is the Task Specific Instruction) in the **configuration phase** (col. 11, line 63, VIM Translation Compacted Type-2 Instructions), wherein the HVLIW contains **a preceding general header** (fig. 1B, header 17/15/13/11), and wherein the HVLIW with **its code-compressed structure** (fig. 5, Store Unit Instructions, Load Unit Instructions, MAU Instructions, DSU Instructions) replaces all functions of the TVLIW; and

a third step that involves, in **an execution phase** (fig. 5, execute units 540/542/544/546/548), executing the HVLIW with its code-compressed structure to actuate the functioning units FUs in the processor, wherein **a Command Code mode** (figs. 6/6A, compacted-2 instruction format mode; and col. 13, lines 32-37) of operation of the HVLIW and its associated general header is implemented so that the general header is followed directly by the first and second FIWs required for constructing the VLIW,

wherein the general header (fig. 1B, header 17/15/13/11) stores the information in coded form, which indicated all combinations regarding which of the first and second FIW instruction word part is provided, after decoding in the execution phase for actuating **a respective first and/or second**

**FU function unit in the processor** (figs. 6A/6B, FUs for SIMD/VLIW style instructions), and

wherein the general header stores which first and/or second FIW take up memory locations in **a cache** (fig. 7A, iVLIW memory VIM 705) and whether or which operations are to be executed with the respective memory content in the execution phase (fig. 6D, such as bits 27-28 for ALU VIM) in the cache when constructing the VLIW.

As to claim 10, Pechanek'592 discloses the method of claim 8, wherein a first part of the general header is provided with a header mode that contains information about the Command Code mode of operation of the HVLIW and of the general header,

wherein the first part is followed by **a second part that stores, coded as table values** (fig. 6B, bits 27-29; as well as bits 12-14), the respective most needed combination regarding which of the respective FUs (fig. 6B, The operating code encoding scheme will determine the actuated functional unit FU at execution time) is actuated by which of the first and second FIW" (fig. 6B), and

wherein a third part is connected as **CE information** (fig. 6B, bits 24-26) and contains a pointer which refers to a provided location in a dictionary, and

wherein the last part of the general header provided is the **supplementary information** (fig. 6B drawing, and col. 13, lines 43-46).

As to claim 11, Pechanek'592 discloses the method of claim 8, wherein **a reference instruction mode** (fig. 7B) of operation of the HVLIW and of the contained general header is implemented in which the FIWs provided for constructing the VLIW in the execution phase are **buffer-stored** (fig. 7B, bits 17-15 (UnitVIM) for the use of buffer-stored cache) in the cache, wherein the associated header mode bears **a correspondingly decodable tag** (fig. 7B, bits 28-25 CtrlOp as a type of instruction opcode field is the decodable tag) for this reference instruction mode of operation,

wherein **the reference instruction mode** (fig. 6B, Group bits bits 31-29 + Instruction bit-23 to make such HVLIW specific to the reference instruction mode) of operation (fig. 7) is initiated by **a specific HVLIW that contains an address statement** (col. 14, lines 16-18) which is used to refer to a reference instruction,

wherein the subsequent HVLIW which likewise bears the tag for the reference instruction mode of operation, contains a relative address for the address statement provided by the

reference (col. 14, lines 18-24, Bits 18-21 specify that up to 16 instructions are to be loaded in the specific functional unit's VIM, indicated by bits 15-17. The instructions begin loading at the address generated by the addition of an address value located in one of two Vb registers, selected by bit-9, plus the VIMOFFS offset address, bits 0-7. The prior art shows the InstrCnt Bits 18-21 as a tag for counting subsequent HVLIW instructions, and the Vb registers can hold addresses.), and

wherein a mask appended to it for the FUs which are to be excluded from the actuation. (col. 14, lines 56-59, The five state d-bits 821, 823, 825, 827, and 829 are LV-loaded disable bits for the instruction slots that indicate either: the instruction slot is available-for-execution or it is not-available-for-execution. The d-bits in the prior art anticipate the "mask" for the functional units FU utilizations.)

As to claim 12, Pechanek'592 discloses the method of claim 11, wherein the address statement of the specific HVLIW which initiates the reference instruction mode of operation refers to **a general address**. (col. 14, lines 16-18, instruction bit-23 that specifies if at least one instruction is to be loaded or if the disable d-bit for the specific address is to be loaded; The

Instruction bit-23 in prior art can specify if a general or a particular address needs to be loaded as "address statement").

As to claim 13, Pechanek'592 discloses the method of claim 8, wherein the execution phase involves the HVLIW being decoded in a decoder which is equipped with a header decoder, a CMDT, a cache and a cache miss repair logic unit, wherein the HVLIW is buffer-stored in the cache, and wherein the header decoder identifies the mode of operation of the general header from the header mode stored therein (col. 10, lines 58-63, in fig. 4A, there are three translate blocks 409/411/413, which allow simple fixed translations to a known state for a given instruction mapping. For example, the group code bits 30 and 31 for the dual compacted instructions 415 are 00, which enable the translation process logic 400. The Translate block 400 which decode group code bits and Translate block 409 are analogous to the claimed "header decoded". The Translate block 411 which decodes operating codes opcode, and Translate 413 are analogous to the CMDT, and the VIM 109 in fig. 1, which anticipates cache and cache, miss repair logic. It is inherently known in the art that the cache has coherency phenomena where a cache replacement as cache repair is always exist.),

wherein the identified header mode is taken as **a basis for decompressing** (col. 10, lines 60-62) the values of the FU-C information which are provided in the general header by means of a comparison with the CMDT and in conjunction with the CE information which is likewise taken from the general header (fig. 4A, 4B, The translate 409/411/413/432 anticipates information translation of the CE, CMDT, and FU-C),

wherein the identified header mode is taken as a basis for processing the supplementary information (col. 10, lines 60-62, The prior art uses examples of the group code bits, in which anticipates header mode to demonstrate the translation process will vary based on its information) in the general header,

wherein possible incorrect access (fig. 1, The VIM 109 which anticipates cache and cache miss repair logic. It is inherently known in the art that the cache has coherency phenomena where a cache replacement, as cache repair, is always exist. After a necessary cache miss recovery, a valid data will be provided at the cache output as result.) during buffer-storage in the cache as cache miss is remedied by the execution of an error handling routine in a cache miss repair logic unit and a valid VLIW is provided at the output of the decoder.

***Response to Arguments***

5. Applicant's arguments filed October 5th, 2007, regarding the 35 U.S.C. §102 have been fully considered, but they are not deemed to be persuasive.

**Applicants argue that Penachek'592 does not disclose amended features in conversion of a TVLIW into HVLIW with a general header that includes FU-combination information on which of the FIWs is to be used for actuating a respective FU in the processor after decoding, as required by claim 8. (page 11, para. 6, lines 2-4).**

Examiner disagrees with Applicants, because Penachek'592 discloses hierarchical conversions of TVLIW to HVLIW and VLIW in figure 5. The general header information is also disclosed in figures 6/6A, such as bits 27-31 and bits 12-14. Penachek'592's general header fields explicitly activate functional units for VLIW style executions after conversions. The decoding and execution operations are also clearly shown in figure 5 as decode/execution units 540/542/544/546/548.

***Conclusion***

6. **This action is made final.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A

shortened statutory period for reply to this final action is set to expire in three months from the mailing date of this action. In the event a first reply is filled within two months of the mailing date of this final action and the advisory action is not mailed until after the end of the three-month shortened statutory period, then the shortened statutory period will expire on the date of the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than six months from the date of this final action.

***Contact Information***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cheng-Yuan Tseng whose telephone number is 571-272-9772, and fax number 571-273-9772. The examiner can normally be reached on 08:00-16:00 Monday-Thursday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on 571-272-4176. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC central telephone number, 571-272-2100. In order to reduce pendency and avoid

potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into the Group at fax number: 703-871-9306. This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

CT
CYT

10/15/07

HENRY TSAI
SUPERVISORY PATENT EXAMINER